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54. Invention Title: Memory Module
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SPECIFICATION

1. TITLE OF INVENTION

Memory Module

2. CLAIMS

1. A memory module that stacks a plurality of semiconductor devices that house individual memory chips and have an electrode pattern at the container outer wall for conducting a chip's electrode to the exterior, and said container outer wall electrode patterns are electrically interconnected.

3. DETAILED DESCRIPTION OF THE INVENTION

Industrial Field of Application

The present invention pertains to a memory module in which a plurality of memory devices is mounted at high density.

In recent years the capacity of memory ICs used in various electronic devices has expanded greatly, and the demand for them continues to increase, year after year.

Prior Art

Memory ICs are typically used as a dual inline package (DIP) sealed by a mold or ceramic case.

Problems the Invention Is to Solve

To increase memory capacity in an electronic device it is necessary to mount as many memory ICs as possible in a limited space, but a DIP-type package requires a relatively large mounting space.

The object of the present invention is to provide a memory module that can mount memory ICs in a limited space at high density.

Means for Solving the Problems

The present invention is characterized as constituting each memory device in a chip carrier system, and vertically stacking a plurality of these.

Embodiment

The details of the present invention are described below with reference to FIG. 1 through FIG. 7.

FIG. 1 shows a circuit that uses four 16k × 8 bit SRAM (Static Random Access Memory) ICs as a circuit that uses memory ICs. As can be seen from this, terminals A_0~A_{10}, IO_1~IO_8, not-W, V_{DD}, GND, and not-CE_2 are wiring that is shared by memory IC 1 through memory IC4; only not-CE_1 is independent for each IC. Utilizing this point, in the present invention terminals 3 are formed at the peripheral surface of the chip carrier as shown in FIG. 2, and these terminals 3 connect to the respective electrodes 2 within the chip carrier.

The peripheral electrodes 3 are disposed so that they overlap the rear-surface electrodes (3 in FIG. 3) of another chip carrier when chip carriers are stacked, so electrical connection is achieved simply by overlapping chip carriers, and [the module] can be miniaturized. Furthermore, 4 is a semiconductor element; this electrode is wire bonded to the chip carrier's internal electrode 2.

FIG. 4 is a sectional view of a chip carrier in accordance with the present invention. It has the electrode 3 for making connections at the carrier periphery and sides, and between chip carriers at the rear surface.

In FIG. 5 an memory IC 4 is mounted on the chip carrier and wired bonded, after which it is sealed by resin 5. If necessary, the chip carrier undergoes a burn-in test and electrical characteristics inspection, and good products are selected.

Good chip carriers have solder 6 supplied to the electrode 3 as shown in FIG. 6.

Next, exactly the required number of chip carriers (4 in the example shown in FIG. 7) are stacked up, and subjected to a solder reflow process, whereby each chip carrier is connected electrically and mechanically, resulting in a memory module.

Furthermore, an electrode that needs to be independent at each IC such as CE_2 may be connected to a different electrode pad at each IC.

Effect of the Invention

As described above, according to the present invention sufficient inspection is performed prior to assembling the chip carriers used into a module, so yield is high and the height of one chip carrier is about 2 mm so stacking even four of them is 8 mm, so [the module] can be greatly miniaturized, etc.

4. BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is an example of a circuit for a memory module that uses four 16k × 8 bit SRAM ICs. FIG. 2 and FIG. 3 are a front view and back view of a chip carrier in accordance with the present invention. FIG. 4 through FIG. 7 are sectional views showing the processes in manufacturing a memory module in accordance with the present invention.

1 Ceramic
2 IC mounting electrode
3 Chip carrier connection electrode
4 Memory IC
5 Sealing resin
6 Solder

Representative: Susumu Uchihara, Patent Agent [seal]

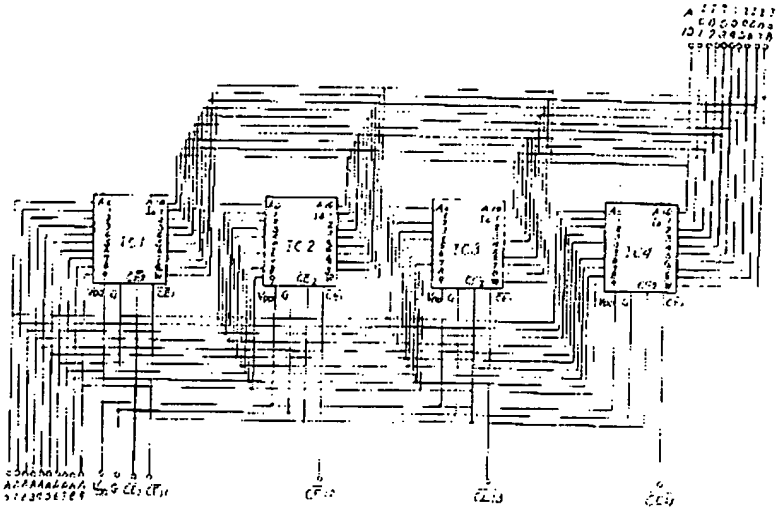

FIG. 1

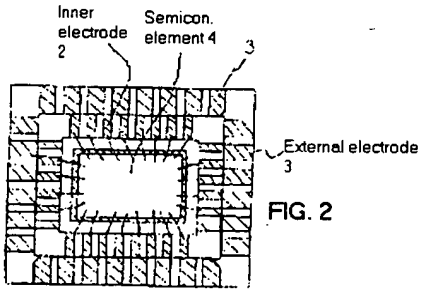

FIG. 2

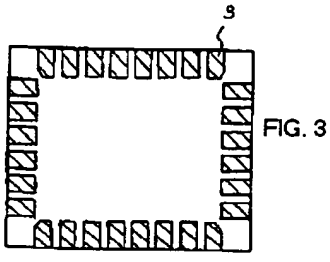

FIG. 3

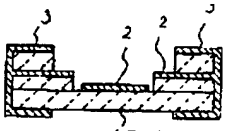

FIG. 4

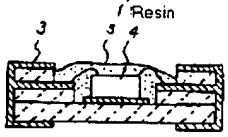

FIG. 5

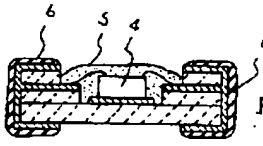

FIG. 6

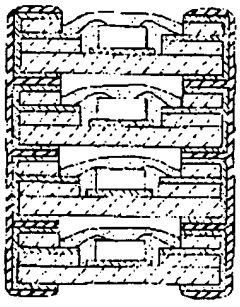

FIG. 7